## CLAIMS

We claim:

1. A read only memory device, comprising:

a read only memory cell array including:

a plurality of first read only memory cells coupled to a plurality of word lines, a plurality of first bit lines, and a plurality of first virtual ground lines; and

a plurality of second read only memory cells coupled to a reference word line, a plurality of second bit lines and a plurality of second virtual ground lines;

a reference memory cell array including:

a plurality of first reference memory cells coupled to a plurality of dummy word lines, at least one reference bit line, and at least one reference virtual ground line; and

at least one second reference memory cell coupled to the reference word line, the at least one reference bit line, and the at least one reference virtual ground line; and

a dummy memory cell array including:

a plurality of first dummy memory cells coupled to the plurality of dummy word lines, at least one dummy bit line, and at least one dummy virtual ground line; and

a plurality of second dummy memory cells coupled to the reference word line, the at least one dummy bit line, and the at least one dummy virtual ground line.

2. The device of claim 1 where the reference word line is selected responsive to the plurality of word lines.

3. The device of claim 1 where the plurality of dummy word lines is coupled to the plurality of word lines.

4. The device of claim 1 where the plurality of dummy word lines is coupled to a power voltage.

5. The device of claim 1 where the plurality of dummy word lines is coupled to a ground voltage.

6. The device of claim 1 where the plurality of dummy word lines is coupled to the plurality of word lines.

7. The device of claim 1

where the plurality of second bit lines is coupled to the plurality of first bit lines; and

where the plurality of second virtual ground lines is coupled to the plurality of first virtual ground lines.

8. The device of claim 1 comprising a MOS transistor having a gate coupled to the reference word line.

9. The device of claim 1 where the read only memory cell array includes an NMOS transistor having a gate coupled to the reference word line.

10. The device of claim 1 where the at least one second reference memory cell includes an NMOS transistor.

11. The device of claim 1 where the at least one second dummy memory cell includes an NMOS transistor.

12. A read only memory device, comprising:

a read only memory cell array including

a plurality of first read only memory cells coupled to a plurality of word lines, a plurality of first bit lines, and a plurality of first virtual ground lines; and

a plurality of second read only memory cells coupled to a reference word line, a plurality of second bit lines, and a plurality of second virtual ground lines;

a reference memory cell array including

a plurality of first reference memory cells coupled to a plurality of dummy word lines, at least one reference bit line, and at least one reference virtual ground line; and

a plurality of second reference memory cells coupled to the reference word line, the at least one reference bit line, and the at least one reference virtual ground line; and

a dummy memory cell array including

a plurality of first dummy memory cells coupled to the plurality of dummy word lines, at least one dummy bit line, and at least one dummy virtual ground line; and

a plurality of second dummy memory cells coupled to the reference word line, the at least one dummy bit line, and the at least one dummy virtual ground line;

a row decoder to decode a row address that selects the plurality of word lines;

a reference word line selecting circuit to select a reference word line responsive to the row address;

a first column decoder and virtual ground line selecting circuit to decode a column address that selects the plurality of bit lines and the plurality of the first virtual ground lines; and

a second column decoder and virtual ground line selecting circuit to select the at least one reference bit line and the at least one dummy bit line responsive to the column address.

13. The device of claim 12 where the reference word line selecting circuit decodes predetermined bits of the row address.